REMARKS

The Office Action dated November 15, 2004 has been received and carefully considered. In this response, claims 1, 11, 15, 16, 19 and 21 have been amended. Support for these amendments may be found in the specification and figures as originally filed. Reconsideration of the outstanding rejections in the present application therefore is respectfully requested based on the following remarks.

Telephonic Interview of February 7, 2005

The undersigned notes with appreciation the courtesies extended by the Examiner during the telephonic interview of February 7, 2005 ("the Interview"). During the Interview, the Applicants' representative proposed amending the independent claims to further include the connection between one or more outputs/output nodes/pins and a memory. The Examiner agreed that the proposed amendments would overcome the rejections of the claims at least for the reasons provided herein.

Anticipation Rejection of Claims 1-5, 8-10, 16, 18, 19 and 21

At page 2 of the Office Action, claims 1-5, 8-10, 16, 18, 19 and 21 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Chang (U.S. Pat. App. Pub. No. 2003/0005247). The claims have been amended, thereby obviating this rejection.

Claim 1, from which claims 2-5 and 8-10 depend, has been amended to recite the limitations of when in a first mode of operation, utilizing a first output *coupled to a memory* to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory.

Claim 16, from which claim 18 depends, has been amended to recite the limitations of an output pin coupled to an output of an address control portion and an output of a first data lane enable control portion, *and further coupled to a memory.*

Claim 19 has been amended to recite the limitations of operational instructions that cause a processing module to utilize a first output *coupled to a memory* to provide a first data lane enable to facilitate accessing of a portion of a first memory storage location of the memory associated with a first memory address when in a first mode of operation and utilize the first output to provide an address bit of a second memory address to facilitate designation of a second memory storage location of the memory when in a second mode of operation.

Claim 21 has been amended to recite the limitations of when the microcomputer is in a first mode of operation, utilizing a first output of a microcomputer to provide a first data lane enable *to a memory* for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and when the microcomputer is in a second mode of operation, utilizing the first output of the microcomputer to provide an address bit of a second memory address *to the memory* for facilitating designation of a second memory storage location of the memory.

The Office Action relies on the SMI#/SMIOUT# output of Chang in support of its rejection of claims 1-5, 8-10, 16, 18, 19 and 21. *Office Action*, pp. 2-3. However, as noted during the Interview and as agreed to by the Examiner, regardless of whether the SMI#/SMIOUT# output of Chang may be properly regarded as a data lane enable, the SMI#/SMIOUT# output connects the CPU 200 and the chipset 220 and is not coupled to the memory 240. Thus, the SMI#/SMIOUT output of Chang is not equivalent to the output/output node/pin of claims 1, 16, 19 and 21. Accordingly, Chang fails to disclose each and every limitation of claims 1, 16, 19 and 21, as well as claims 2-5, 8-10 and 18 at least by virtue of their dependency from one of claims 1 or 16. Moreover, these claims recite additional limitations that are not disclosed by Chang.

Accordingly, it is respectfully submitted that the anticipation rejection of claims 1-5, 8-10, 16, 18, 19 and 21 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejections of Claims 6, 11-15, 17 and 20

At page 5 of the Office Action, claims 6, 11-15, 17 and 20 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang and the Microsoft Computer Dictionary. At page 7 of the Office Action, claim 17 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang and the Authoritative Dictionary of IEEE Standard Terms. The claims have been amended, thereby obviating this rejection.

Claim 1, from which claim 6 depends, has been amended to recite the limitations of when in a first mode of operation, utilizing a first output *coupled to a memory* to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory.

Claim 16, from which claim 17 depends, has been amended to recite the limitations of an output pin coupled to an output of an address control portion and an output of a first data lane enable control portion, *and further coupled to a memory.*

Claim 19, from which claim 20 depends, has been amended to recite the limitations of operational instructions that cause a processing module to utilize a first output *coupled to a memory* to provide a first data lane enable to facilitate accessing of a portion of a first memory storage location of the memory associated with a first memory address when in a first mode of operation and utilize the first output to provide an address bit of a second memory address to facilitate designation of a second memory storage location of the memory when in a second mode of operation.

As noted above, Chang fails to disclose or suggest the limitations of an output/output pin coupled to a memory as recited by claims 1, 16 and 19. Likewise, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to provide any disclosure related to these limitations. Accordingly, the proposed combinations of Chang, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to disclose or suggest each and every limitation of claims 6, 17 and 20 at least by virtue of their dependency from claims 1, 16 and 19, respectively.

Claim 11, from which claims 12-14 depend, has been amended to recite the limitations of A method of providing data to a set of pins of a device, *the set of pins coupled to a memory*, the method comprising: during a first mode of operation, multiplexing a first set of data onto the set of pins to allow the set of pins to provide data representing two least significant bits of a first address, a most significant bit of the first address, and a lane enable, during a second mode of operation, multiplexing a second set of data onto the set of pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address, and two lane enables, and during a third mode of operation, multiplexing a third set of data onto the set of pins to allow the set of pins to provide four lane enables.

As similarly noted above with respect to claims 1, 16, 19 and 21 and as agreed to by the Examiner, the SMI#/SMIOUT# output connects the CPU 200 and the chipset 220 and is not coupled to the memory 240. Thus, the SMI#/SMIOUT output of Chang is not equivalent to the limitations of a set of pins coupled to memory as recited by claim 11. Likewise, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to provide any disclosure related to these limitations. Accordingly, the proposed combinations of Chang, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to disclose or suggest each and every limitation of claim 11, as well as claims 12-14 at least by virtue of their dependency from claim 11. Moreover, these claims recite additional limitations that are not disclosed by Chang or the other cited references.

Claim 15 has been amended to recite the limitations of a set of address nodes *coupled to a memory* to provide address data for address bit locations A(n) through A(2), where A(n) represents a most significant bit for at least a first mode of operation, a first output node *coupled to the memory* to provide one of an address data for address bit location A(1) and a data lane enable signal based upon a mode of operation, a second output node *coupled to the memory* to provide one of an address data for address bit location A(0) and a data lane enable signal based upon the mode of operation, a third output node *coupled to the memory* to provide one of an address data for address bit location A(n+1) and a data lane enable signal based upon the mode of operation.

As similarly noted with respect to claims 1, 16, 19 and 21 and as agreed to by the Examiner, the SMI#/SMIOUT# output connects the CPU 200 and the chipset 220 and is not coupled to the memory 240. Thus, the SMI#/SMIOUT output of Chang is not equivalent to the first and second outputs of claim 15. Likewise, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to provide any disclosure related to these limitations. Accordingly, the proposed combinations of Chang, the Microsoft Computing Dictionary and the Authoritative Dictionary of IEEE Standard Terms fail to disclose or suggest each and every limitation of claim

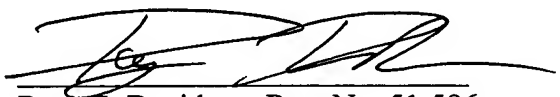
Accordingly, it is respectfully submitted that the obviousness rejections of claims 6, 11-15, 17 and 20 are improper at this time and withdrawal of these rejections therefore is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

8 February 2005
Date

Respectfully submitted,



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